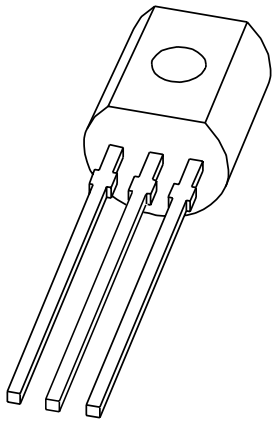
DATA SHEET



PDTA144ES
PNP resistor-equipped transistor

Product specification
Supersedes data of 1997 Jul 01
File under Discrete Semiconductors, SC04

1998 May 19

Philips
Semiconductors

PHILIPS

PNP resistor-equipped transistor PDTA144ES

FEATURES

- Built-in bias resistors R1 and R2 (typ. 47 kΩ each)
- Simplification of circuit design
- Reduces number of components and board space.

APPLICATIONS

- Especially suitable for space reduction in interface and driver circuits
- Inverter circuit configurations without use of external resistors.

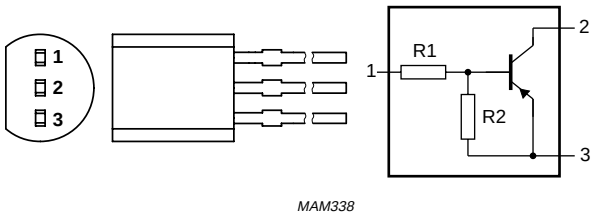


Fig.1 Simplified outline (TO-92; SOT54) and symbol.

DESCRIPTION

PNP resistor-equipped transistor in a TO-92; SOT54 plastic package.
NPN complement: PDTC144ES.

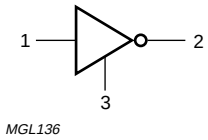


Fig.2 Equivalent inverter symbol.

PINNING

PIN	DESCRIPTION
1	base/input
2	collector/output
3	emitter/ground (+)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CEO}	collector-emitter voltage	open base	–	–	–50	V
I_O	output current (DC)		–	–	–100	mA
I_{CM}	peak collector current		–	–	–100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	–	–	500	mW
h_{FE}	DC current gain	$I_C = -5$ mA; $V_{CE} = -5$ V	80	–	–	
R1	input resistor		33	47	61	kΩ
$\frac{R2}{R1}$	resistor ratio		0.8	1	1.2	

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	–50	V
V_{CEO}	collector-emitter voltage	open base	–	–50	V
V_{EBO}	emitter-base voltage	open collector	–	–10	V
V_I	input voltage				
	positive		–	+10	V
	negative		–	–40	V
I_O	output current (DC)		–	–100	mA
I_{CM}	peak collector current		–	–100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	500	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–65	+150	°C

Note

1. Transistor mounted on an FR4 printed-circuit board.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	250	K/W

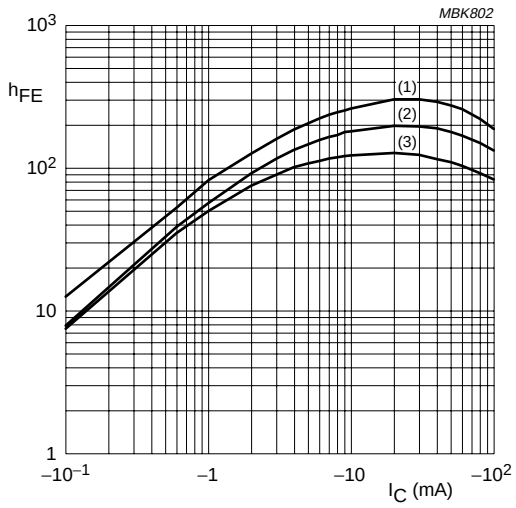
Note

1. Transistor mounted on an FR4 printed-circuit board.

CHARACTERISTICS

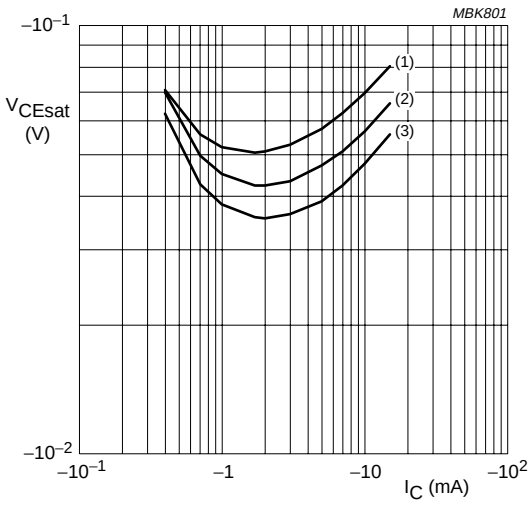
T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector cut-off current	$I_E = 0$; $V_{CB} = –50$ V	–	–	–100	nA
I_{CEO}	collector cut-off current	$I_B = 0$; $V_{CE} = –30$ V	–	–	–1	µA
		$I_B = 0$; $V_{CE} = –30$ V; $T_j = 150$ °C	–	–	–50	µA
I_{EBO}	emitter cut-off current	$I_C = 0$; $V_{EB} = –5$ V	–	–	–90	µA
h_{FE}	DC current gain	$I_C = –5$ mA; $V_{CE} = –5$ V	80	–	–	
V_{CEsat}	collector-emitter saturation voltage	$I_C = –10$ mA; $I_B = –0.5$ mA	–	–	–150	mV
$V_{i(off)}$	input-off voltage	$I_C = –100$ µA; $V_{CE} = –5$ V	–	–1.2	–0.8	V
$V_{i(on)}$	input-on voltage	$I_C = –2$ mA; $V_{CE} = –0.3$ V	–3	–1.6	–	V
R1	input resistor		33	47	61	kΩ
$\frac{R2}{R1}$	resistor ratio		0.8	1	1.2	
C_c	collector capacitance	$I_E = i_e = 0$; $V_{CB} = –10$ V; f = 1 MHz	–	–	3	pF



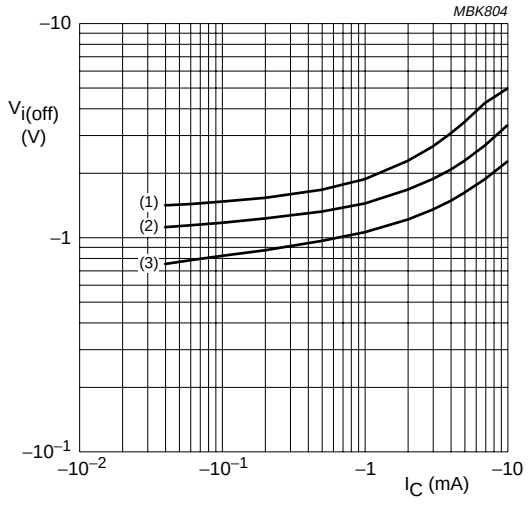
V_{CE} = –5 V.
(1) T_{amb} = 150 °C.
(2) T_{amb} = 25 °C.
(3) T_{amb} = –40 °C.

Fig.3 DC current gain as a function of collector current; typical values.



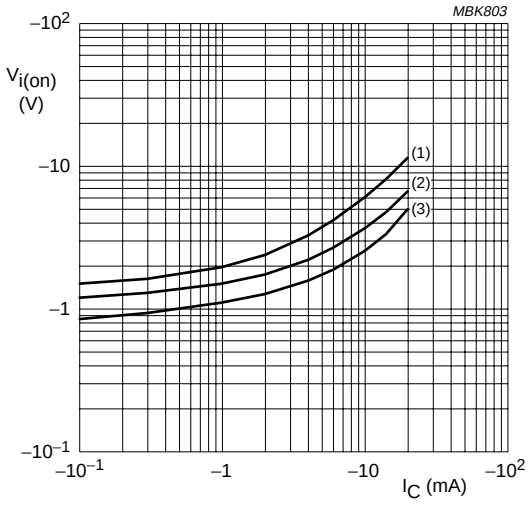
I_C/I_B = 20.
(1) T_{amb} = 100 °C.
(2) T_{amb} = 25 °C.
(3) T_{amb} = –40 °C.

Fig.4 Collector-emitter saturation voltage as a function of collector current; typical values.



V_{CE} = –5 V.
(1) T_{amb} = –40 °C.
(2) T_{amb} = 25 °C.
(3) T_{amb} = 100 °C.

Fig.5 Input-off voltage as a function of collector current; typical values.

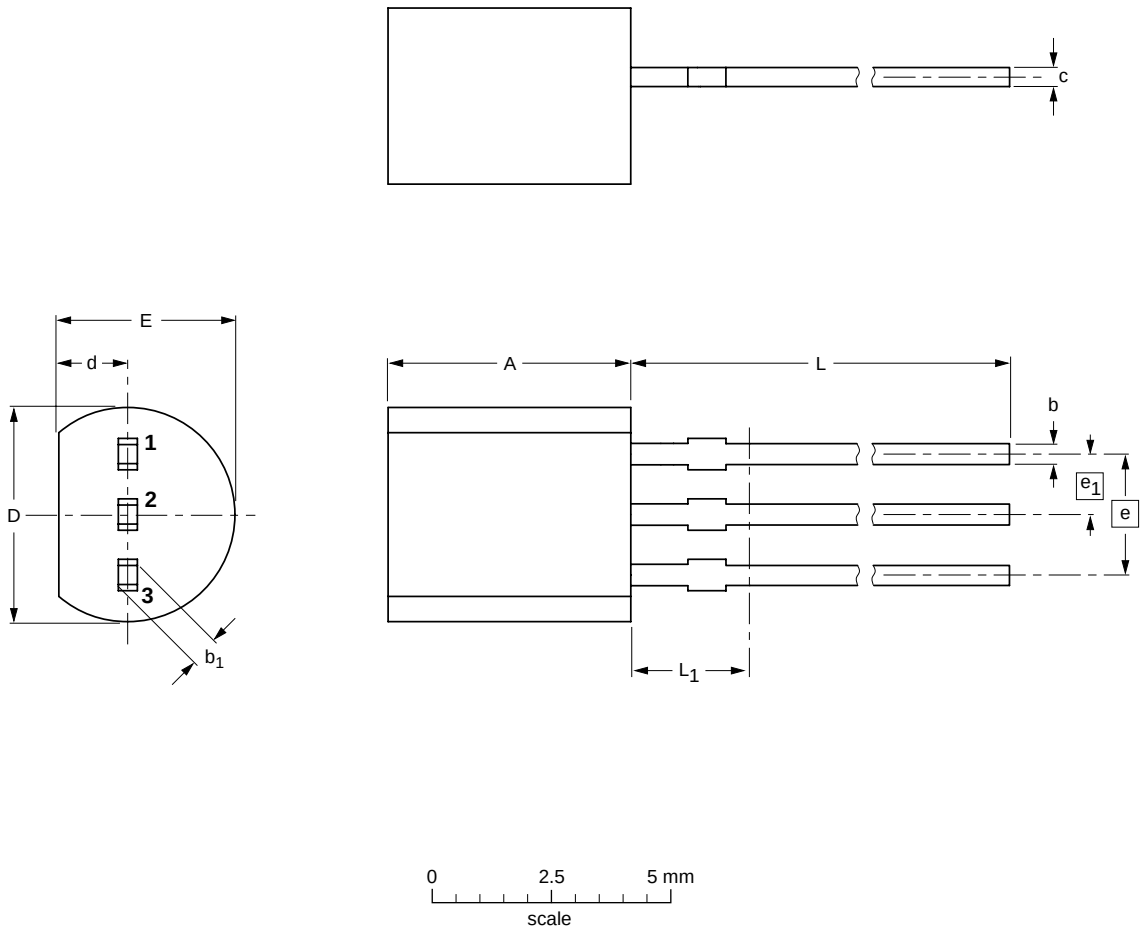


V_{CE} = –0.3 V.
(1) T_{amb} = –40 °C.
(2) T_{amb} = 25 °C.
(3) T_{amb} = 100 °C.

Fig.6 Input-on voltage as a function of collector current; typical values.

PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; 3 leads **SOT54**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b_1	c	D	d	E	e	e_1	L	L_1(1)
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT54		TO-92	SC-43			97-02-28

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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